ELECTRICAL AND THERMAL PROCESSES IN TEMPERATURE-LIMITED TRANSISTORS

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A study is made of the interrelation between electrical and thermal processes in temperature-limited transistors. The results of theoretical analysis are compared with experimental data.

One promising way to make power transistors suitable for operation as switches is to use temperature-limited transistors for this purpose. The gist of temperature limitation is establishment, through a critical thermistor in direct thermal contact with the semiconductor wafer, of a feedback between the temperature of the structure and the collector current of the transistor which will cause the current to decrease as the structure heats up to its critical temperature T_{cr}. Temperature limitation makes it feasible to operate power transistors as switches characterized by a high reliability and noncritical with respect to current overloads. The behavior of a temperature-limited transistor in this mode of operation is determined by a combination of electrical and thermal processes, which in this kind of device are fundamentally interrelated. The object of this study is to analyze the interrelation between those processes.

The structure of a temperature-limited transistor in the most general form includes a semiconductor (silicon) wafer whose upper surface and lower surface are in thermal contact with, respectively, the critical thermistor and the heat sink. The electrical circuit of a temperature-limited transistor can generally have any configuration. Here will be considered a conventional transistor stage with a common-emitter connection (Fig. 1). The critical thermistor Rp is connected in a series before the input and a dc voltage V_C is applied to the collector. Such a mode of operation occurs during a short circuit across the load and is most severe with respect to the necessary fast response of the thermal protection (temperature limiter). An analysis of temperature transducers indicates that with silicon devices it is appropriate to use a PTC (positive temperature coefficient) thermistor Rp as a critical one. The temperature dependence of its electrical resistance has been described in other studies [1, 2] and can be approximated by the relation

$$R_p = R_0 + R_d \{\exp[\gamma(\Theta_p - \Theta_{cr})] - 1\}. \quad (1)$$

Passage of a collector current through the transistor generates a power P in the silicon wafer and dissipation of this power causes the wafer to heat up. Owing to the inertia of a PTC thermistor, the instantaneous temperature of the silicon wafer can appreciably exceed the critical temperature T_{cr} when power P rises fast to a high level. Accordingly, it is of practical interest to determine the maximum temperature reached by the structure in the temperature-limitation mode when a step of power P = const impinges on the temperature-limited transistor. Solution of this problem involves a composite analysis of electrical and thermal processes in the transistor.

The thermal processes will be analyzed under the following assumptions: the thermal circuit of a temperature-limited transistor is regarded as a one-dimensional stack of diverse plates in thermal contact with one another, and the density of the power dissipated in this transistor is uniform over the upper surface of the silicon wafer.

The electrical processes will be analyzed under the following assumptions: voltage u_C at the reverse-biased collector junction is much higher than the voltage at the forward-biased emitter junction, with the power dissipated in the temperature-limited transistor

$$p = u_c i_c; \quad (2)$$

The electrical processes within the structure reach the steady state much sooner than the thermal processes do, so that they can be regarded as quasisteady ones, which makes it permissible to use the static characteristics of a transistor.

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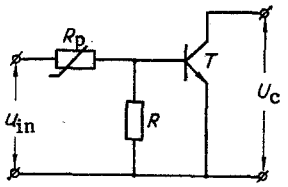

Fig. 1. Transistor stage with a common-emitter connection: PTC thermistor R_p, resistor R, temperature-limited transistor T.

The dependence of the dissipated power on the PTC resistance $p(r_p)$ is known, this dependence being determined by the transistor circuit connection, and its trend can be established either by experiment or by calculation. When the base circuit of the transistor stage in Fig. 1 is supplied from a source of base current $i_b = u_{in}/r_p$, this base current being related to the collector current by the equality $i_c = \beta i_b$, then the relation $p(r_p)$ can be expressed as

$$p(r_p) = u_c \beta u_{in}/r_p. \tag{3}$$

In a transistor without temperature limitation the dissipated power p depends only on the electrical operating parameters. In order to calculate the temperature rise $\vartheta(t)$ of the structure (in the plane of power generation) for any form of the power as a function of time p(t), therefore, it is sufficient to determine the transient thermal resistance of the transistor $r_T(t)$ numerically equal to the temperature rise of the structure due to a unit step of power. Then

$$\vartheta(t) = p(0)\, r_T(t) + \int_0^t r_T(t-\xi)\, p'(\xi)\, d\xi. \tag{4}$$

In a temperature-limited transistor p(t) depends not only on the electrical operating parameters but also on the temperature of the PTC thermistor. For calculating the thermal modes of temperature-limited transistors, therefore, one must not only know the transient thermal resistance $r_T(t)$ of the transistor proper but also have available a family of transient thermal resistances in various cross sections of the PTC thermistor $r_{TP}(x, t)$ numerically equal to the temperature rises in corresponding cross sections of the thermistor due to a unit step of power in the transistor. It will be demonstrated here that determining the transient thermal resistance $r_{TP}(x, t)$ of a PTC thermistor reduces to determining the thermal resistance $r_T(t)$ and the transfer function, with respect to temperature, of the PTC thermistor $y_P(x, t)$. This transfer function represents the response of a PTC thermistor to a unit step of temperature in the plane of the upper surface of the silicon wafer. The general equation for the temperature rise of a PTC thermistor is

$$\vartheta_p(x, t) = \vartheta(0)\, y_p(x, t) + \int_0^t y_p(x, t-\xi)\, \vartheta'(\xi)\, d\xi. \tag{5}$$

Considering that $\vartheta(0) = 0$ and $\vartheta(t) = Pr_T(t)$, we obtain

$$\vartheta_p(x, t) = P \int_0^t y_p(x, t-\xi)\, r_T'(\xi)\, d\xi$$

and from here

$$r_{Tp}(x, t) = \frac{\vartheta_p(x, t)}{P} = \int_0^t y_p(x, t-\xi)\, r_T'(\xi)\, d\xi. \tag{6}$$

Relations $r_T(t)$ and $r_{TP}(t)$ are determined by the design of the device and can be established either by calculation or by experiment.

We will now consider the steady-state operation of a temperature-limited transistor. The power dissipated in the transistor will be expressed in terms of its steady-state thermal resistance R_T and the temperature rise of the PTC thermistor Θ_p, the latter in the steady state equal to the temperature rise of the transistor Θ in the plane of power generation: $P = \Theta_p/R_T$. On the other hand, the same power can be represented as a function of the electrical resistance of the PTC thermistor R_P and the latter is in turn a function of its temperature rise Θ_P: $P = P[R_P(\Theta_P)]$. We thus arrive at the equation which determines the steady-state temperature rise of the structure in the temperature-limitation mode

$$\Theta_p/R_T = P[R_p(\Theta_p)]. \tag{7}$$

As an example, let us calculate the steady-state performance of a temperature-limited transistor in a common-emitter circuit (Fig. 1). Inserting the relation $P(R_P)$ from expression (3) into the right-hand side of Eq. (7) yields

$$\frac{\Theta_p}{R_T} = \frac{U_c \beta U_{in}}{R_p(\Theta_p)}. \tag{8}$$

With the aid of the temperature dependence (1) of the electrical resistance of the PTC thermistor, we can reduce Eq. (8) to

$$\frac{\Theta_p}{R_T} = \frac{P_0}{1 + \frac{R_d}{R_0}\{\exp[\gamma(\Theta_p - \Theta_{cr})] - 1\}}. \tag{9}$$

The quantity $P_0 = U_c \beta U_{in}/R_0$ represents the power step acting on the "cold" device under conditions preceding the temperature limitation ($\vartheta_P \leq \Theta_{cr}$).

We can now calculate the steady-state performance of a temperature-limited transistor with the parameters $R_T = 10°C/W$, $T_{cr} = 75°C$, $R_0 = 42\ \Omega$, $R_d = 1\ \Omega$, and $\gamma = 0.21\ (°C)^{-1}$ on which impinges a step of power $P_0 = 1000$ W. Let the ambient temperature T_0 be equal to the critical temperature so that $\Theta_{cr} = T_{cr} - T_0 = 0$ in one case, and equal to zero so that $\Theta_{cr} = T_{cr}$ in the other case. In the first case $\Theta_P = 46°C$, $T = T_P = \Theta_P + T_0 = 121°C$, and $P = 4.6$ W. In the second case $\Theta_P = 116°C$, $T = T_P = 116°C$, and $P = 11.6$ W. This example illustrates that, despite the rather large step of power P_0, the steady-state temperature of the structure $T = T_P$ in the temperature-limitation mode remains far below the maximum allowable 150°C, while the steady-state dissipated power P is below the initial level P_0.

We next consider the transient performance of a temperature-limited transistor. Knowing the temperature dependence $\rho_P(T_P)$ of the electrical resistivity of the PTC thermistor and knowing the thickness l_P as well as the cross-sectional area σ_P of the PTC thermistor, we can write for its total resistance, which depends on the space distribution of its temperature $T_P(x, t)$,

$$r_p = \frac{1}{\sigma_p} \int_0^{l_p} \rho_p [T_p(x, t)]\, dx. \tag{10}$$

With the aid of relation (10), the dependence of the power on the electrical resistance of the PTC thermistor $p(r_P)$ can be transformed to the dependence $p[T_P(x, t)]$. This dependence obviously determines the inverse relation $T_P(x, t) = f[p(t)]$ for the absolute temperature and the relation $\vartheta_P(x, t) = \varphi[p(t)]$ for the temperature rise above the initial temperature of the PTC thermistor. With $\vartheta_P(x, t)$ now represented according to relation (4), where $r_T(t)$ is replaced by $r_{TP}(x, t)$, the integral equation for the power with the argument in an implicit form becomes

$$p(0)\, r_{TP}(x, t) + \int_0^t r_{TP}(x, t - \xi)\, p'(\xi)\, d\xi = \varphi[p(t)]. \tag{11}$$

After determining the function $p(t)$ from expression (11), we calculate the temperature rise of the silicon wafer according to relation (4).

Another approach is analogous to the one taken for calculating the steady-state performance. The transform of power dissipated in the structure will be expressed in terms of the transform of temperature rise $\Theta_P(x, s)$ and the transient thermal resistance $R_{TP}(x, s)$ of the PTC thermistor, namely,

$$P(s) = \Theta_p(x, s)/R_{TP}(x, s). \tag{12}$$

On the other hand, the transform of power can be expressed as the Laplace integral of the function on the right-hand side of Eq. (7)

$$P(s) = \mathcal{L}\{p[r_p(\vartheta_p)]\} = \mathcal{L}\{p[\vartheta_p(x, t)]\}. \tag{13}$$

Equating the transforms of power (12) and (13), then applying the multiplication theorem for transforms, we obtain an integral equation for the temperature rise of the PTC thermistor

$$\vartheta_p(x, t) = \int_0^t r_{TP}(x, t - \xi)\, p[\vartheta_p(x, \xi)]\, d\xi. \tag{14}$$

Considering that the transform of power (12) can be analogously expressed in terms of the transform of temperature rise $\Theta(s)$ of the silicon wafer and the transient thermal resistance $R_T(s)$ of the transistor proper, we can find the quantity $\Theta(s)$ as

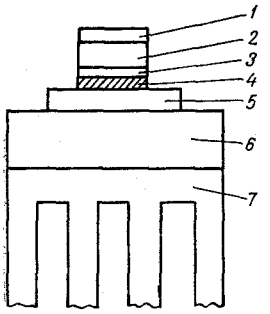

Fig. 2

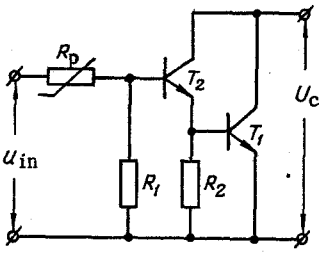

Fig. 3

Fig. 2. Construction of a temperature-limited transistor: 1) PTC thermistor (barium titanate); 2) insulating plate (beryllium oxide); 3) adhesive layer (epoxide); 4) silicon wafer; 5) thermal compensator (molybdenuum); 6) copper case; 7) aluminum radiator.

Fig. 3. Transistor stage connected into a Darlington circuit: PTC thermistor R_P; resistors R_1 and R_2; temperature-limited transistor T_1; auxiliary transistor T_2.

$$\Theta(s) = \frac{\Theta_P(x, s)}{R_{TP}(x, s)} R_T(s). \tag{15}$$

An inverse transformation of the quantity (15) yields $\vartheta(t)$.

The results of calculations by this method, pertaining to the transient processes in a temperature-limited transistor, have been compared with experimental data. The test object was a temperature-limited transistor of a construction as shown in Fig. 2. So as to avoid errors due to heating of the PTC thermistor by the input current, the test device was connected into a Darlington circuit (Fig. 3). Since the purpose of the experiment was to validate the proposed method of calculation rather than developing recommendations for optimal design of temperature-limited transistors, all relations in the fundamental equations were, as a rule, determined experimentally. These relations were then either approximated by sufficiently accurate analytical expressions or used directly in numerical integration. This made it possible to avoid laborious calculations based on electrothermophysical equations and inevitable errors of theoretical assumptions.

The transient thermal resistance $r_T(t)$ of the transistor was measured by the well-known experimental method, using the forward voltage drop across the emitter junction as the heat-sensitive parameter at a constant measuring current.

Experimental determination of $r_{TP}(x, t)$ is fraught with great difficulties. For this reason, the transient thermal resistance $r_{TP}(x, t)$ of the PTC thermistor was calculated by numerical integration of Eq. (6). Use was made of the experimentally determined $r_T(t)$ relation together with the calculated $y_P(x, t)$ function. For calculating the latter, the system of equations of heat conduction was solved for plates 1 and 2, with plate 3 regarded as a thermal contact resistance. Inasmuch as the thermal capacity of the insulating layer 2 between the silicon wafer and the PTC thermistor was appreciably higher than that of the PTC thermistor, values of function $y_P(x, t)$ almost did not vary along the x coordinate. Therefore, the transfer function $y_P(t)$ was calculated with respect to the mean-over-the-volume temperature of the PTC thermistor. The $r_{TP}(t)$ relation over the $0 \leq t \leq 10$ sec range, obtained as a result of numerical integration, was subsequently approximated as

$$r_{TP}(t) = b_1 t + c\,[1 - \exp(-b_2 t)], \tag{16}$$

with $b_1 = 0.08$°C/W, $b_2 = 0.55$ sec^{-1}, and $c = 1$°C/W.

The temperature dependence of the electrical resistance of the PTC thermistor, established experimentally, was approximated by Eq. (1) with $R_0 = 42\ \Omega$, $R_d = 1\ \Omega$, and $\gamma = 0.2$ (°C)$^{-1}$. This relation was then used in numerical integration directly, without prior conversion according to expression (10). This was justified by the fact that during the heating process the temperature almost did not vary across the thickness of the PTC thermistor, owing to the large thermal capacity of the insulating layer 2.

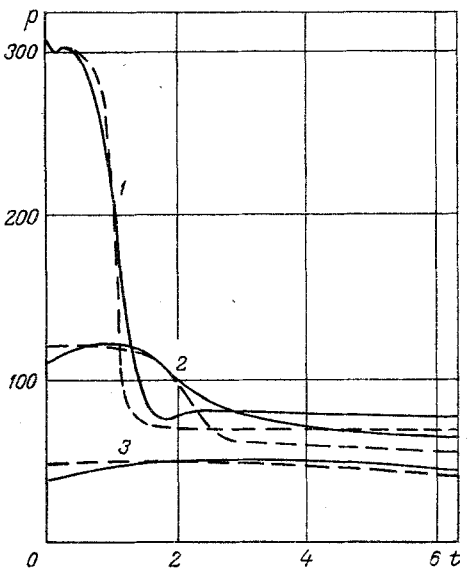

Fig. 4. Dissipated power p (W) as a function of time t (sec), calculated (dash lines) and measured (solid lines) for various values of P_0: 1) 300 W; 2) 120; 3) 50.

The dependence of the power dissipated in the temperature-limited transistor on the electrical resistance of the PTC thermistor, established experimentally, was approximated as a linear function $p(r_P) = P_0[1 - k(r_P - R_0)]$, with $k = 0.003\ (\Omega)^{-1}$. The dependence of the temperature rise of the PTC thermistor on the dissipated power, established with the aid of relation (1), could then be reduced to the relation

$$\vartheta_P(t) = \frac{1}{\gamma} \ln \frac{P_0(1 + kR_d) - p(t)}{P_0 kR_d} + \Theta_{cr}. \tag{17}$$

Inserting $r_{TP}(t)$ from (16) and $\vartheta_P(t)$ from (17) into Eq. (11), then applying the differentiation theorem for the convolution of two functions, we now obtain an equation for the power dissipated in a temperature-limited transistor

$$p'(t) = \gamma c b_2 [P_0(1 + kR_d) - p(t)] \left\{ \frac{1}{\gamma c} \ln \frac{P_0(1 + kR_d) - p(t)}{P_0 kR_d} + \frac{\Theta_{cr}}{c} - p(t) \left(1 + \frac{b_1}{cb_2} \right) - \frac{b_1}{c} \int_0^t p(\xi)\, d\xi \right\}. \tag{18}$$

Results of numerically solving Eq. (18) for various values of the acting power P_0 are shown in Fig. 4 (dashed lines). On the same diagram are also shown experimental curves (solid lines) which have been plotted according to the following procedure. The temperature-limited transistor was hit by a step of power $P_0 = U_C I_{C0}$ varying with the collector current I_{C0}, inasmuch as the collector–emitter voltage was held constant (U_C = const). The variation of the collector current $i_C(t)$ and thus also the variation of the power $p(t) = U_C i_C(t)$ were recorded with a loop oscillograph.

According to the graphs in Fig. 4, the agreement between theoretically and experimentally established relations is entirely satisfactory, not only with respect to the trend but also with respect to the orders of magnitude. This confirms the correctness of the proposed method and of the assumptions made here.

NOTATION

t, instantaneous time; x, space coordinate in a cross section of the PTC thermistor; $F(x, s) = \mathcal{L}[f(x, t)]$ Laplace integral transform of function f(x, t); T_0, ambient temperature; T, steady-state temperature of the transistor in the plane of power generation; T_P, steady-state temperature of the PTC thermistor; T_{cr}, critical temperature of the PTC thermistor; $\Theta = T - T_0$, steady-state temperature rise of the transistor in the plane of power generation; $\Theta_P = T_P - T_0$, steady-state temperature rise of the PTC thermistor; $\Theta_{cr} = T_{cr} - T_0$, critical temperature rise of the PTC thermistor; ϑ, instantaneous temperature rise of the transistor in the plane of power generation; ϑ_P, instantaneous temperature rise of the PTC thermistor; P, steady-state dissipated power; p, instantaneous dissipated power; P_0, step of dissipated power corresponding to $\vartheta_P(x, t) \leq \Theta_{cr}$;

R_T and r_T, steady-state and the transient thermal resistance of the transitor in the plane of power generation; R_{TP} and r_{TP}, steady-state and the transient thermal resistance of the PTC thermistor; y_P, transfer function of the PTC thermistor with respect to temperature; U_C and u_C, dc and the instantaneous collector voltage in the transistor circuit; U_{in} and u_{in}, dc and the instantaneous input voltage to the transistor stage; I_{C0}, dc collector current in the transistor corresponding to $\vartheta(x, t) \leq \Theta_{cr}$; i_C, instantaneous collector current; i_b, instantaneous base current; R_P and r_P, steady-state and the instantaneous electrical resistance of the PTC thermistor; γ, R_0, R_d, parameters of the resistance-temperature characteristic of the PTC thermistor; ρ_P, electrical resistivity of the PTC thermistor; σ_P, cross-sectional area of the PTC thermistor; l_P, thickness of the PTC thermistor in the x direction; and β, a, k, c, b_1, b_2, coefficients.

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CALCULATION OF A TRANSIENT IN A TWO-POLE NETWORK WITH A THERMISTOR

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An analytical expression is derived which describes the variation of the thermistor temperature during a relay-effect transient process following an instantaneous change in the supply voltage in an $R - R_T$ two-pole network.

Thermistors, a widely known class of semiconductor devices, can be successfully used in various relay and pulse devices utilizing the electrothermal relay effect. This effect takes place when a dc voltage is applied to the input of two-pole network containing a thermistor and a linear resistor [1-5].

The transient process in such a network will be described by the well-known differential equation [1]

$$C_V \frac{dT}{dt} = \frac{E^2 R_\infty \exp(B/T)}{[R_\infty \exp(B/T) + R]^2} - H(T - T_a). \quad (1)$$

This equation can be easily reduced to quadratures by separation of variables, but the resulting expression in terms of elementary function is not integrable. For this reason, several methods of simplifying the fundamental equation (1) have been developed so as to yield a solution. These include linearization of the differential equation (1), assuming small deviations of thermal and electrical parameters in the network, the method of piecewise-linear approximation [3], replacement of the thermistor with an equivalent two-pole network [4], graphical integration [5], etc. However, these methods either are applicable to only a narrow temperature range or require special graph plotting without being universal and convenient.

In this study, based on a set of assumptions about the characteristics of electrothermal processes in a thermistor, an attempt will be made to simplify Eq. (1) and to solve it in an analytical form.

For the construction of a workable physical model describing the processes of charge transfer in a thermistor, we will utilize the fact that the current–voltage characteristic of a thermistor has a typical, for it, range of negative resistance. The physical processes occurring in semiconductor devices with such a characteristic are conveniently described with the aid of models which utilize concepts pertaining to a so-called hot gas of charge carriers [6].

Let us examine the process of current flow in a thermistor on the basis of these concepts. After a voltage has been applied to the input of a four-pole network containing a thermistor and a linear resistor, the

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